# Mid-term Examination - Semiconductor devices II – Spring 2023 (prof. Ionescu)

## Questions on theory

Select by a **CIRCLE**, ONE or MORE correct answers for each of the questions below.

Each good answer is marked by +1, each wrong answer is marked by -1

Even if not mandatory, you can motivate your answer under 'Comments'.

**Question 1**: **Technology Boosters for field effect transistors**

The nanometer CMOS performance advancement is enabled by **technology boosters** (by definition, a technology innovation that improves some of the device performance in static and/or dynamic operation). Some of these technology boosters can be also extended to other devices such as Tunnel FETs or Negative Capacitance FETs.

Select the correct statements concerning such performance boosters.

1. Use of **Germanium material in the channel or source** architecture is **not a technology booster** for **both** Tunnel FETs and MOSFETs (p-type).
2. **Tensile strain** can be considered a technology booster for both MOSFETs and Tunnel FETs.
3. A **very thin channel resulting in a Fully Depleted (FD) semiconducting film is a technology booster** for both MOSFETs and NC MOSFETs because it reduces the leakage and junction capacitance of source and drain junctions.
4. The **Gate-All-Around (GAA) transistor architecture** is **not** a technology booster for FETs and Tunnel FETs.
5. **Scaling the channel length** is a technology booster with similar scaling advantage on performance improvement for both Tunnel FETs and MOSFETs.
6. **Scaling the channel width** is a technology booster for both Tunnel FETs and MOSFETs.
7. **A junctionless transistor architecture** is a technology booster for MOSFETs.
8. There is **no known practical technology booster** for **scaling the power density** together with the dimensional scaling in MOSFETs.
9. High-k dielectrics and a multi-gate transistor architecture are **additive technology boosters for Tunnel FETs, MOSFETs and NC MOSFETs.**
10. **Negative capacitance** in itself **is a technology booster** for MOSFETs and not really a novel device principle, from the point of view of channel carrier conduction mechanism.

Comments on Question 1:

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**Question 2: Metal-Insulator-Transition (MIT) switches**

The Metal-Insulator-Transition (MIT) switches can be considered as a steep slope switch exploiting the phase change in some functional oxides, that can cover applications

Choose the correct properties of MIT switches from the below statements.

1. In a three terminal MIT switch, with an insulating gate control over a $VO_2$ material channel, **the challenge consists in having the steep transition OFF-ON at a low level of current and low gate voltage**.
2. The **mechanism of switching** the current in a MIT switch corresponds **to reversible a change from an amorphous phase (low insulator) to a crystalline phase (conductive)** of the material structure.
3. $VO_2$ is a **rare and toxic material**, so it needs particular care in the fabrication processes in the clean room.
4. The **switching mechanism in $VO_2$ two-terminal switch** from OFF to ON state turns a CAPACITOR to a RESISTOR, from an electrically equivalent circuit point of view, which mean this mechanism can be potentially used to designed reconfigurable RF devices.
5. The **bandgap of the $VO_2$ switch** in the OFF state (insulating) **dictates the Ioff** current in a 3-terminal switch configuration.
6. The $VO_2$ switch has a subthreshold swing between OFF and ON states that is **nearly proportional with kT/q**.
7. A VO2 switch has **transition times (OFF to ON and ON to OFF)** typically **much smaller** that micrometer site MEMS switches.
8. The switching mechanism in $VO_2$ switches is hysteretic; this is enabling **memristive applications such as mimicking the function of a neuron synapse**.
9. The mechanism used in $VO_2$ switches as pressure or gas sensors is the **modulation of the electrical conductivity after the gas adsorption**.

10. By doping $VO_2$ with Germanium **both transition thresholds (MIT and IMT) are reduced** towards lower-than-68°C temperature.

Comments on Question 2:

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**Question 3: Critical comparison of MIT (VO2) switches, Tunnel FET switches and fully depleted (FD) SOI MOSFET switch.**

A. Enumerate four (4) **advantages** of MIT (VO2) switch compared to a Tunnel FET
B. Enumerate four (4) **disadvantages** of a Tunnel FET compared to a SOI MOSFET switch.
C. Enumerate **three (3) electronic applications** taking the full advantage of the most promising figures of merit of the MIT (VO2), Tunnel FET and FD SOI MOSFET.

**A)**

1)

2)

3)

4)

**B)**

1)

2)

3)

4)

**C)**

1) Applications MIT (VO2) switch:

2) Applications Tunnel FET switch:

3) Applications FD SOI FET switch :